PATENT APPLICATION
DOCKET NO.: 200209002-1

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Original) A match circuit for implementation in a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the match circuit comprising logic for activating a match signal when a selected *N*-bit portion of the debug data matches an *N*-bit threshold for all bits selected by an *N*-bit match mask ("mmask").

2. (Original) The match circuit of claim 1 wherein *N* is equal to sixteen.

3. (Original) The match circuit of claim 1 wherein the *N*-bit threshold is provided from a control status register ("CSR").

4. (Original) The match circuit of claim 1 wherein the *N*-bit mmask is provided from a control status register ("CSR").

5. (Original) The match circuit of claim 1 wherein the debug data comprises 80 bits.

6. (Original) The match circuit of claim 5 wherein the debug data comprises eight 16-bit portions aligned on 10-bit blocks.

7. (Original) The match circuit of claim 6 wherein the selected portion comprises one of the eight 16-bit portions.

8. (Original) The match circuit of claim 1 wherein the logic for activating a match signal comprises logic for comparing a binary bit of the selected debug data portion with a corresponding bit of the threshold and outputting a binary bit indicative of whether the compared bits match.